1. (15%) An amplifier with an input resistance of 100 kΩ and an output resistance of 1 kΩ is to be capacitor-coupled to a 10-kΩ source and 1-kΩ load. Available capacitors have values only of the form 1×10^{-n} F. What are the values of the smallest capacitors needed to ensure that the corner frequency associated with each is less than 100 Hz?
2. (10%) Why is the bandwidth of a cascade amplifier larger, in general, than that of a simple common-emitter amplifier?
3. (10%) An op amp having a slew rate of 20 V/μs is to be used in the unity-gain follower configuration, with input pulses that rise from 0 to 3V. What is the shortest pulse that can be used while ensuring full-amplitude output?
4. (15%) Design an inverting op-amp circuit with a voltage gain of $A_v = v_O / v_I = -30$ and an input resistance that is the largest value possible but under the constraint that the largest resistance value is limited to 1 MΩ.
5. (15%) It is required to design a non-inverting amplifier with a dc gain of 10. When a step voltage of 100 mV is applied at the input, it is required that the output be within 1% of its final value of 1 V in at most 100 ns. What must the f_t (unity-gain bandwidth) of the op amp be?
6. (10%) Describe a two-input NMOS OR logic circuit.
7. (10%) A common-gate amplifier using an *n*-channel enhancement MOS transistor for which transconductance $g_m = 5$ mA/V has a 5-kΩ drain resistance (R_D) and a 2-kΩ load resistance (R_L). The amplifier is driven by a voltage source having a 200-Ω resistance. What is the input resistance of the amplifier?
8. (15%) When the collector of a transistor is connected to its base, use the simplified hybrid-π model to find the incremental (small-signal) resistance of the resulting two-terminal device.

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