1. For the high-frequency model of an NMOS device in Fig. 1, neglect the channel modulation effect and body effect. Please write three kinds of formulas for the transconductance in terms of some of $I_D$, $V_{OV}$, W/L, $\mu_n$, *and* $C_{ox}$ (9%)
2. For the high-frequency model of an NMOS device in Fig. 1, please write its transition frequency (3%). Supposed $C_{gs} >> C_{gd}$ and $C_{gs} \simeq \frac{2}{3}WLC_{ox}$, how to double this transition frequency in terms of the channel length, L, only (3%)
3. For a cascade current mirror in Fig. 2, neglect the channel modulation effect and the body effect. Assume the aspect ratio of all the NMOS devices is $W/L$. To have all the NMOS devices in saturation, please write the minimal output voltage, Vo, (5%) in terms of $I_{REF}$, $V_T$, W/L, $\mu_n$, *and* $C_{ox}$.
4. For a differential pair in Fig. 3, please write three sources to induce the input offset voltage (5%). Owing to these three sources, please write the common-mode rejection ratio if the output voltage is taken single-endedly (5%).
5. Please write five properties if the negative feedback is applied to an amplifier (5%).
6. For the 741 op-amp circuit in Fig. 4, explain the following questions:
   (a) What are the purposes of Q3 and Q4. (6%), (b) What is the purpose of Q7 (2%)
   (c) What is the short-circuit protection circuitry (4%), (d) What is the purpose of Q23 (3%)

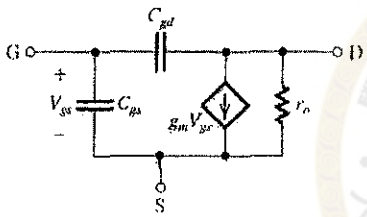


Fig. 1

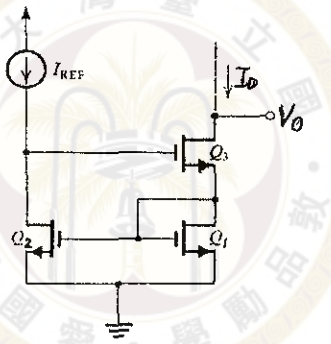


Fig. 2

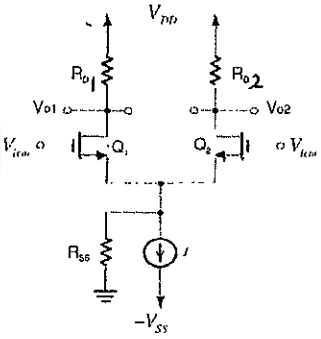


Fig. 3

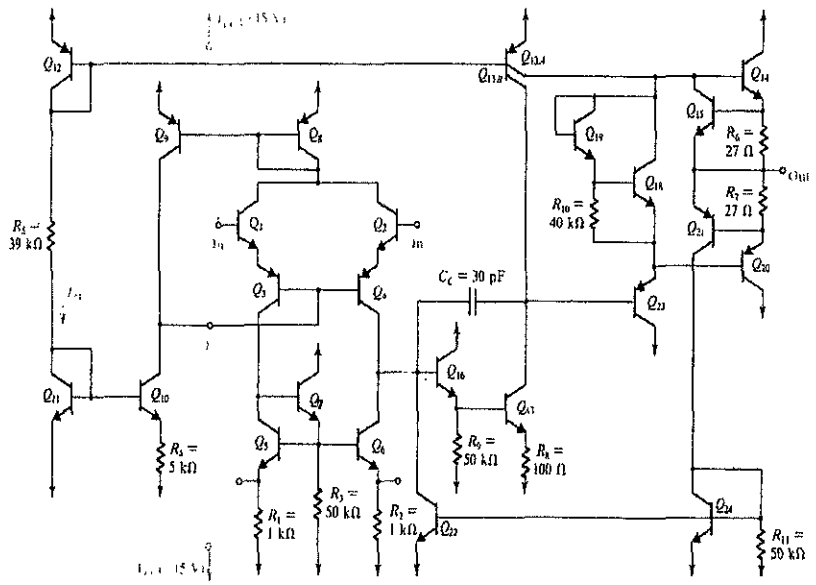


Fig. 4

7. (a) Use ***Complementary Pass-transistor Logic (CPL)*** to implement the logic function, $S = ABC + A\overline{B}\overline{C} + \overline{A}B\overline{C} + \overline{A}\overline{B}C$, and its complement, $\overline{S}$. Please draw your design at the transistor level, assuming all the inputs $A, B, C, \overline{A}, \overline{B}, \overline{C}$, are available. (9%)
(b) Assume that the threshold voltages of NMOS and PMOS transistors are 0.45 V and -0.43V, respectively. If $A, B, C$, are set to 1.5 V, and $\overline{A}, \overline{B}, \overline{C}$ are set to 0 V, determine the voltage levels of all the nodes in your design. (6%)

8. (a) Please design a first-order high-pass filter with only passive components. (3%)
(b) What is the transfer function of the filter in (a)? (3%)
(c) Please draw the pole-zero pattern on the s-plane for the filter in (a). (3%)
(d) Please draw the transmission characteristics of the filter in (a). (3%)
(e) Please design a first-order high-pass filter using one OP-Amp and passive components. (3%)
(f) What is the transfer function of the filter in (e)? (3%)
(g) Why active-RC filters are less popular in monolithic ICs? (3%)

9. (a) What is the mechanism of ***drift current*** in semiconductors? (4%)
(b) Please explain what ***recombination*** process is in semiconductors. (6%)
(c) What is ***Common-Mode Rejection Ratio***? (4%)

試題隨卷繳回