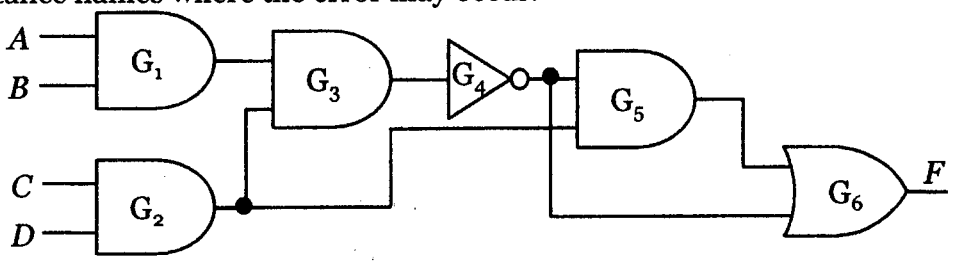
1. (16%) Consider the following logic circuit. According to the specification, with applying the input vector (A, B, C, D) = (0, 0, 1, 1), the output value at F should be 0. However, the actual simulation result is 1. Assume the error is caused by using wrong gate types, and only three possibilities are considered: AND↔NAND, OR↔NOR, Inverter↔Buffer (one buffer equals two cascaded inverters). If a single error occurs, please write down the possible gate instance names where the error may occur.



2. (16%) Consider a 4-input function.

$$f(A, B, C, D) = AC + AB'C' + BC'D.$$

   (a) (8%) Apply Shannon expansion theorem to iteratively expand f on A, B, C, D (in order). Write down the fully expanded function f.
   (b) (6%) Use 2-to-1 multiplexors to implement f obtained in (a), where A, B, C, D can only be select signals.
   (c) (2%) Redo (b) with the minimum number of 2-to-1 multiplexors.

3. (18%) Given the following map of cell locations, we want to group the eight cells, a, b, ..., g, h, into two sets, so that *adjacent* cells belong to different sets. Two cells, i and j, are *adjacent* if $|x_i-x_j| \le 1$ and $|y_i-y_j| \le 1$, where x_i and y_i are the x-coordinate and y-coordinate of cell i, respectively. Let $g_i = 0$ and $g_i = 1$ denote cell i belonging to groups 1 and 2, respectively.

4	a			b
3		c	d	
2	e			f
1		g	h	
coordinate	1	2	3	4

   (a) (8%) Express the above cell grouping problem in terms of a product-of-sums (POS) formula (Boolean Expression without simplification) such that the formula can be satisfied if and only if the cells in the given map can be grouped as desired.
   (b) (6%) How many solutions are there to the formula of (a)? Write down all the solutions if there is any.
   (c) (4%) Rewrite the formula of (a) in a minimum sum-of-products (SOP) expression.

4. (16%) An M-N flip-flop has two inputs $\{M, N\}$ and two outputs $\{Q, Q'\}$. It behaves as follows:
   If MN = 11, the next state of output (Q^+) is 0.
   If MN = 10, the next state of output is the same as the present state.
   If MN = 01, the next state of output is 1.
   If MN = 00, the next state of output is the complement of the present state.
   (a) (4%) Complete the following table for M, N.

Present state Q	Next state Q^+	M	N
0	0		
0	1		
1	0		
1	1		

   (b) (4%) Use your answer in (a) to derive the characteristic (next state) equation for this flip-flop. (i.e., express Q^+ in terms of M, N and Q).
   (c) (4%) Implement an M-N flip-flop based on T flip-flop.
   (d) (4%) Write down the minimum SOPs of the next-state equations for both flip-flops in the following circuit. A^+=? B^+=?

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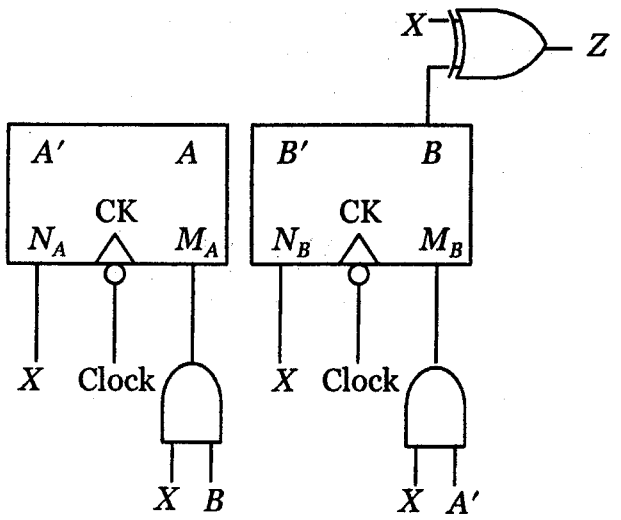
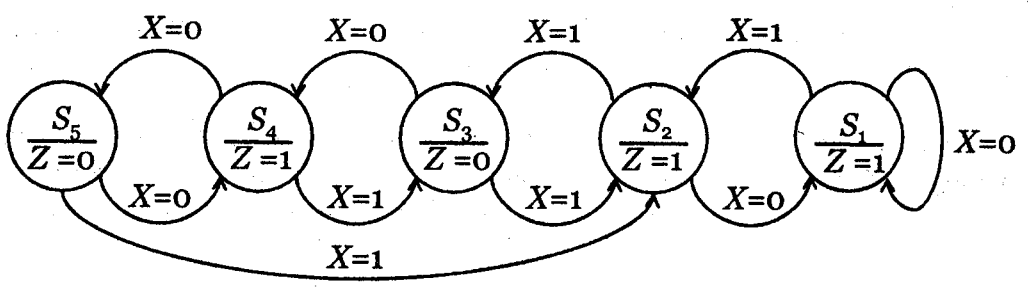


5. (16%) Consider the following state graph.

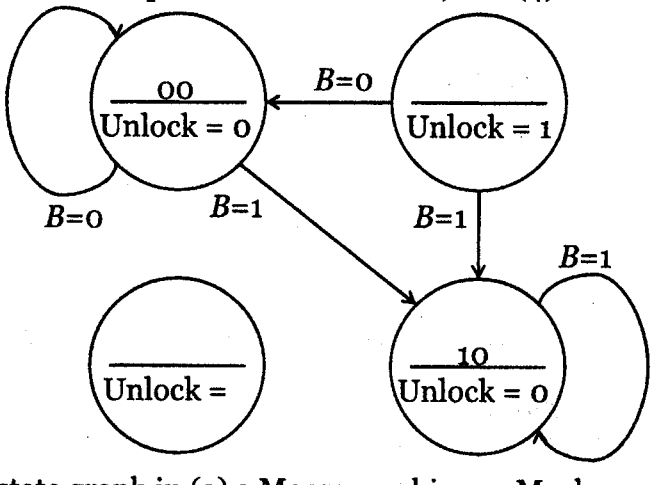


(a) (10%) Simplify the given state graph with input X and output Z. Draw the simplified state graph with minimum states.

(b) (6%) Implement the state graph in (b) using D flip-flops based on one-hot state assignment, which allocates one flip-flop for each state. Give the output function and all flip-flop input equations.

6. (18%) Sophie is designing a digital padlock for her treasure case. The padlock has two buttons ('0' and '1') that when pressed cause the finite state machine (FSM) controlling the padlock to advance to a new state. In addition to advancing the FSM, each button press is encoded on the B signal (B=0 for button '0', B =1 for button '1'). The padlock unlocks when the FSM sets the Unlock output signal to 1, which it does whenever the last N button presses are the same as the preset N-digit code.

(a) (12%) Unfortunately the design notes for the padlock are incomplete. Using the specification above and clues gleaned from the partially completed graphs below, please help Sophie to complete the state graph and its transition table. (Fill in the missing information.)
Please note that when done, (1) each state in the state graph should be assigned a 2-bit sequence Q_1Q_0 (note that in this design the state assignment is not derived from the code that opens the padlock), (2) the arcs (lines with arrows) leaving each state should be mutually exclusive and collectively exhaustive, (3) the value for Unlock should be specified for each state, and (4) the transition table should be completed.



Q_1Q_0	$Q_1^+Q_0^+$ B = 0	$Q_1^+Q_0^+$ B = 1	Unlock
00	00	10	
01	11		0
10	01		
11			1

(b) (2%) Is the state graph in (a) a Moore machine or Mealy machine?

(c) (4%) What is the code that opens the padlock?

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