※ 注意：請於試卷內之「非選擇題作答區」作答，並應註明作答之題號。

1. Choose ALL correct statements from the following: [5%]

   (a) For a CMOS inverter with $(W/L)_N = (W/L)_P$, the propagation delay is given as $t_{PLH} > t_{PHL}$.

   (b) The static power dissipation of a CMOS inverter is proportional to the operating frequency.

   (c) The dynamic power dissipation of a CMOS inverter is independent of the transistor size.

   (d) The switching threshold of a matched CMOS inverter depends on the size of the transistors.

   (e) For a CMOS inverter, NM_H increases as $(W/L)_N$ increases.

2. Choose ALL correct statements from the following: [5%]

   (a) A latch circuit has two stable states.

   (b) The static power dissipation of 6T CMOS SRAM cells is 0.

   (c) SRAM is a non-volatile memory.

   (d) DRAM is a non-volatile memory.

   (e) The read operation of a SRAM cell has to be nondestructive.

3. Consider the amplifier circuit as shown in Fig. 3. The parameters are given as $\mu_n C_{ox}(W/L) = 2\ mA/V^2$, $V_t = 1\ V$, $V_{DD} = 10\ V$, $R_D = 8\ k\Omega$, $R_G = 1\ M\Omega$, $R_L = 4\ k\Omega$, $R_s = 100\ k\Omega$ and the coupling capacitors (C_{C1} and C_{C2}) are ideal.

   (a) Draw the midband small-signal equivalent circuit and find the voltage gain (v_o/v_s). [10%]

   (b) Find the input resistance (R_{in}) of the amplifier. [5%]

   (c) It is obvious that the gain depends on the value of R_G. How do you choose R_G to achieve a voltage gain of -4? [5%]

   (d) In order to evaluate the high-frequency response of the circuit, please draw the small-signal equivalent circuit by including C_{gs} and C_{gd}. [5%]

   (e) Given that $C_{gs} = 200\ fF$ and $C_{gd} = 50\ fF$, use time constant method to evaluate the 3-dB frequency of the amplifier. [10%]
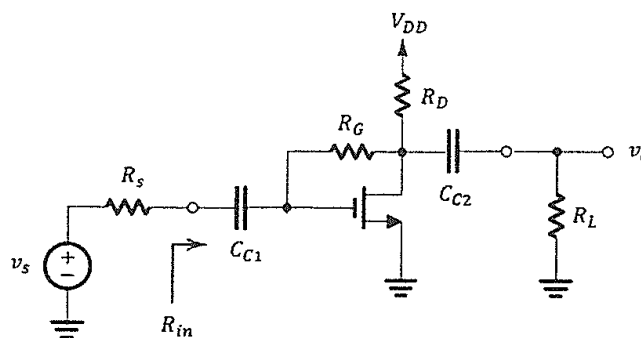

Fig. 3

4. Assume the op-amp is ideal in Fig. 4.

   (a) Derive the transfer function $T(s) \equiv V_o/V_i$ of the circuit. [10%]

   (b) For $m = 2$, find the magnitude and phase of the transfer function at $\omega = 1/RC$. [5%]

   (c) To ensure no gain peaking in the frequency response, how do you choose the design parameter m? [5%]
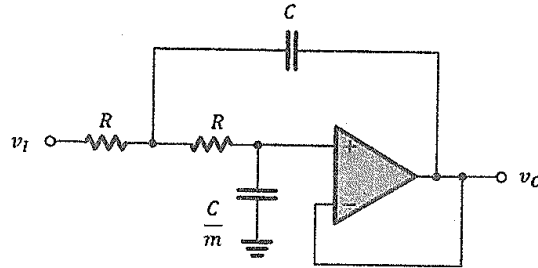
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Fig. 4

5. The schematic and small-signal equivalent circuit of a two-stage op amp are shown in Fig. 5(a) and (b), respectively. Assume the magnitude of early voltage V_A is identical for all MOSFETs. The circuit parameters are specified as $C_C = 10C_2$, $C_2 \gg C_1$ and $\left(\frac{W}{L}\right)_6 = k\left(\frac{W}{L}\right)_3$.

(a) In order to avoid systematic output dc offset, find the ratio of $\left(\frac{W}{L}\right)_7$ and $\left(\frac{W}{L}\right)_5$. [5%]

(b) Based on the small-signal equivalent circuit in Fig. 5(b), derive the low-frequency gain, unity-gain frequency (ω_t). Also find the frequencies of the dominant pole (ω_{P1}), the second pole (ω_{P2}) and the zero (ω_Z). [10%]

(c) It is found that $\omega_t = \omega_Z$ for $k = 1$. Calculate the phase margin of the op-amp for $k = 2$. [10%]
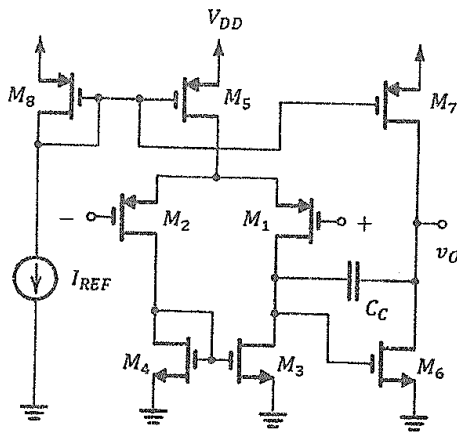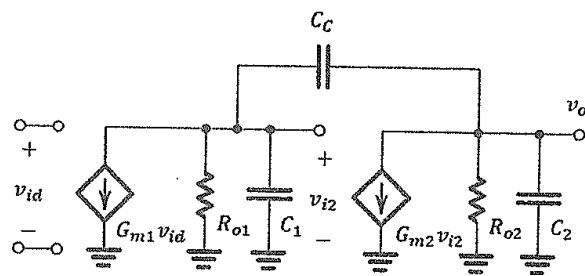

Fig. 5(a)

Fig. 5(b)

6. For the digital circuit in Fig. 6, the NMOS transistor M_1 is used as a pass-transistor login, which passes logic level from V_X to V_Y. Assume $V_{DD} = 1.8\,V$, $\mu_n C_{ox}(W/L) = 1\,mA/V^2$, $V_t = 0.5\,V$, and the parasitic capacitance $C = 100\,fF$. In consideration of the body effect, the threshold voltage of the NMOS device can be specified as $V_t = 0.5 + 0.4\left(\sqrt{0.7 + V_{SB}} - \sqrt{0.7}\right)V$.

(a) For $V_X = 0\,V$ and $V_Y = 1.8\,V$, find the charging current through M_1. [2%]

(b) For $V_X = 0\,V$ and $V_Y = 0.9\,V$, find the charging current through M_1. [2%]

(c) Based on the charging currents in (a) and (b), please evaluate the propagation delay t_{PHL}. [1%]

(d) For $V_X = 1.8\,V$ and $V_Y = 0\,V$, find the charging current through M_1. [2%]

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(e) For $V_X = 1.8\,V$ and $V_Y = 0.9\,V$, find the charging current through M_1. [2%]

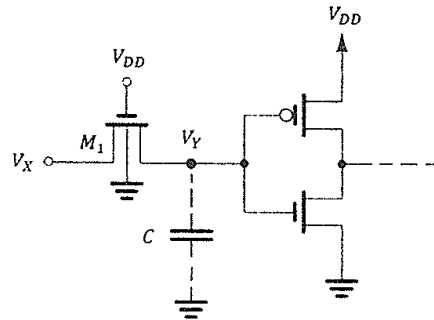(f) Based on the charging currents in (d) and (e), please evaluate the propagation delay t_{PLH}. [1%]

Fig. 6

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